

**"FEE ADDRESS" INDICATION FORM**

To: MAIL STOP: M Fee Correspondence  
U.S. Patent & Trademark Office  
P.O. Box 1450  
Alexandria, VA 22313-1450

Please recognize as the "Fee Address," under the provisions of 37 CFR 1.363, the following address:

COMPUTER PATENT ANNUITIES, INC.  
225 Reinekers Lane  
Suite 400  
Alexandria, VA 22314

Payor Number: 000197

in the following listed application(s) or patent(s) for which the issue fee has been paid.

<u>Patent No.</u>	<u>Serial No.</u>	<u>Patent Date</u>	<u>US Filing Date</u>	<u>Confirmation No.</u>	<u>Attorney Docket No.</u>
7,405,033B2	10/757,193	07/29/2008	01/14/2004	3577	0553-0394

Respectfully Submitted,



Mark J. Murphy  
Registration No. 34,225  
Date: September 23, 2008

COOK ALEX Ltd.  
200 West Adams Street  
Suite 2850  
Chicago, Illinois 60606  
(312) 236-8500

Customer No: 26568



US007405033B2

(12) **United States Patent**  
**Yamazaki et al.**

(10) **Patent No.:** **US 7,405,033 B2**  
 (45) **Date of Patent:** **Jul. 29, 2008**

(54) **METHOD FOR MANUFACTURING RESIST PATTERN AND METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE**

(75) Inventors: **Shunpei Yamazaki**, Tokyo (JP);  
**Yasuyuki Arai**, Atsugi (JP); **Yasuko Watanabe**, Atsugi (JP)

(73) Assignee: **Semiconductor Energy Laboratory Co., Ltd.** (JP)

(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 610 days.

(21) Appl. No.: **10/757,193**

(22) Filed: **Jan. 14, 2004**

(65) **Prior Publication Data**  
 US 2004/0147066 A1 Jul. 29, 2004

(30) **Foreign Application Priority Data**  
 Jan. 17, 2003 (JP) ..... 2003-009111

(51) **Int. Cl.**  
**G03F 7/20** (2006.01)  
**G03F 7/26** (2006.01)  
**G03F 7/16** (2006.01)

(52) **U.S. Cl.** ..... **430/311; 430/394; 430/322**

(58) **Field of Classification Search** ..... **430/311, 430/394**

See application file for complete search history.

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

5,132,248 A	7/1992	Drummond et al.	437/173
5,380,670 A *	1/1995	Hagino	438/138
6,294,401 B1	9/2001	Jacobson et al.	438/99
6,362,507 B1	3/2002	Ogawa et al.	257/350
6,514,801 B1	2/2003	Yudasaka et al.	438/151
6,713,389 B2 *	3/2004	Speakman	438/674

6,794,220 B2	9/2004	Hirai et al.	438/99
2002/0070382 A1	6/2002	Yamazaki et al.	
2002/0197565 A1 *	12/2002	Wu	430/311
2003/0054653 A1	3/2003	Yamazaki et al.	438/694
2003/0059987 A1	3/2003	Sirringhaus et al.	438/149
2003/0202132 A1 *	10/2003	Park	349/43
2004/0121264 A1 *	6/2004	Liegl et al.	430/311
2004/0134420 A1 *	7/2004	Lei	118/50
2004/0147066 A1	7/2004	Yamazaki et al.	
2004/0147113 A1	7/2004	Yamazaki et al.	438/660
2004/0253835 A1	12/2004	Kawase	438/780
2005/0032378 A1 *	2/2005	Yu et al.	435/689

(Continued)

**FOREIGN PATENT DOCUMENTS**

JP 05-338187 12/1993

(Continued)

*Primary Examiner*—Mark F. Huff

*Assistant Examiner*—Brittany Raymond

(74) *Attorney, Agent, or Firm*—Cook, Alex, McFarron, Manzo, Cummings & Mehler, Ltd.

(57) **ABSTRACT**

To provide a method for manufacturing a resist pattern designed to reduce a manufacturing cost by improving efficiency in the use of a resist material, a method for removing a resist pattern, and a method for manufacturing a semiconductor device.

The present invention includes a step of forming a resist pattern by discharging a composition containing photosensitizer on a object to be processed under reduced pressure. The present invention includes a step of etching the object to be processed using the resist pattern as a mask, a step of irradiating the resist pattern through a photomask with light within a photosensitive wavelength region of a photosensitizer, and a step of removing the resist pattern on the object to be processed.

**22 Claims, 16 Drawing Sheets**

